



An FPGA-Based Emulation Platform For Optical-Enabled System

CPU + IO FPGA 仿真平台

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New Focus for Intel Labs China: Advanced Research in Embedded Systems



Embedded Systems Research

Embedded
Connected
Embedded
Systems
Software
Software
Architecture

Electronic HW/SW Design

Intel[®] Technologies
Cores, SoC Building Blocks, Video Analytics co-processors,
MeeGo*, SW Tools, ...

Agenda

- Design challenges
- Evaluation methods
- Our approach
- Implementation
- Q&A



Design challenges

- Besides the well-known issues:
 - Memory wall
 - Power wall
 - Frequency wall
 - SW productivity
- We must make the system
 - Balanced
 - I/O, CPU and interconnection
 - Efficient
 - Cost, performance







Evaluation methods

Simulation

- Pros: flexible, cost effective, fast turnaround
- Cons: slow, insufficient model accuracy

• Emulation:

- Pros: flexible, speed, model accuracy, convincing result
- Cons: HW resource limited, difficult to scale
- Hybrid-simulation







Our view and approach

- More and more BW required
 - HD video, data sharing, video conference....
- Electrical cable approaching physical limitation
 - Eye closes at ~10Gbps data rate on FR4 board *
- I/O will be the next focus for optical technology penetration
 - Discrete chips can be used
 - Optical on-die integration not mature yet
 - Intel announced LightPeak to simplify I/O design

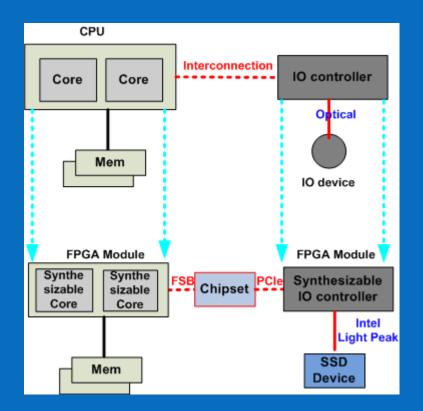






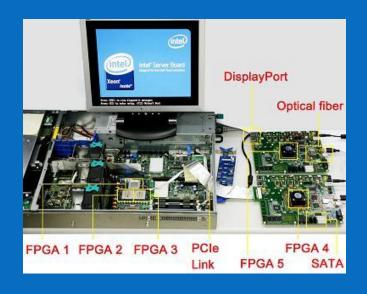
Our view and approach (Cont.)

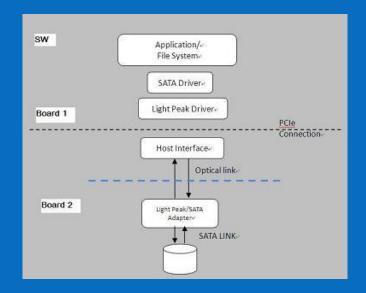
- I/O throughput increased to 10+Gbps enabled by optical
 - IO controller? Special offloading engine?
 - Interconnection?
 - uArch of the cores?
 - HW/SW partitioning?
- Research platform needed to explore the huge design space!
- We adopt FPGA emulation approach and implement core and IO controller in FPGA
 - Flexibility to changes both IO and core





The Implementation





- SATA SSD as the IO device
- The data and control path: SATA SSD and LPK controller
 ⇔optical fiber ⇔ LPK to PCIe transformer ⇔ PCIe cable ⇔ motherboard and core



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